Dielectric and Copper CMP - the Evolution of Integrated Process Control and Solutions Down to 65nm and below

By
Dr. Moshe Finarov, Mr. Avron Ger, Dr. Giora Dishon
Nova Measuring Instruments Ltd., Rehovoth, Israel

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Abstract

Integrated metrology has been first introduced into the production process of semiconductor manufacturing in dielectric CMP in 1995. The new and immature CMP process, the highest COO step, required fast and cost effective incorporation into manufacturing, which helped proving the viability of integrated metrology as a production tool. From the thick dielectric CMP of up to 8 metal layers (down to 0.13um technology node), through advanced STI polishing with angstrom thick residues, to very complex copper polishing with very sensitive low-K and cap layers (65nm and below), integrated metrology has evolved in measurement capabilities, performance and advanced control mechanisms, to provide real time process control needs. Integrated metrology will continue to evolve with 2D metrology capabilities in the CMP process control for 45nm and below with of complex stacks and materials.

CMP Integrated Metrology (IM) History at a Glance

The chemical mechanical planarization (CMP) market is one of the fastest growing technology areas within the semiconductor industry. With equipment and materials revenues estimated at more than $1 billion in 1999, this combined market is slated to exceed $2.4 billion by 2005 (Fig. 1). In the early nineties, when oxide CMP was penetrating into semiconductor manufacturing, the process suffered from significant instabilities and non-uniformities, requiring rigorous process control.

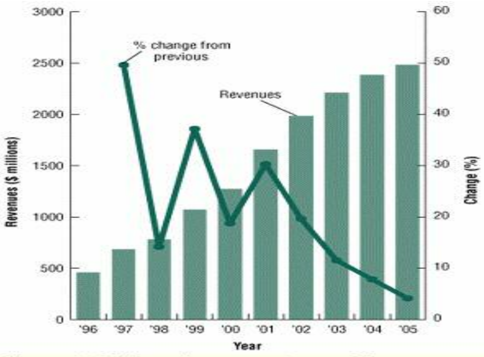


Figure 1. CMP equipment and materials revenues.

Two main elements constituted process control as practiced by all advanced semiconductor manufacturers:

1. Very high sampling of the oxide thickness of the polished layers (more than 5 wafers per lot).
2. The “Gating” method: polish first wafer, clean, dry and measure – then feedback the result to adjust the process for the consecutive wafers in the lot.

The first generation polishers were designed as “dry in – wet out” tools, and required cleaning and drying the polished wafers with a separate cleaner prior to measurement on a stand-alone thin-film metrology tool. This procedure took many hours and led to very low CMP equipment efficiency (much less than 50%). The best way to overcome was to install the metrology system inside the polishing equipment.

The major challenge was the incorporation of a stand-alone compatible, high-accuracy, large-sized and very sensitive optical measurement system inside the process tool environment, which is characterized by mechanical vibrations, electromagnetic interference and water ambient. Moreover, since the polished wafers were kept in water (until removed, cleaned and dried), it was necessary to carry out the optical measurements in water, something that was not practiced before. Integrating a high precision system with the processing equipment required a metrology tool with higher reliability and higher throughput, so not to affect the polisher's uptime and throughput. In addition, high tool-to-tool matching of the metrology was needed in order to provide uniform metrology criteria for all polishers in the fab.

In Semicon West '95 show, July 1995, Nova Measuring Instruments presented the first commercial ITM (Integrated Thickness Monitoring) system, the NovaScan 210. The system with its dedicated, compact opto-mechanical design met all above-mentioned requirements, while keeping the wafer stationary and in water during measurement [8]. The system was designed for accurate thickness measurement of dielectric films and stacks (as needed in multilevel interconnects) inside the polisher, and was integrated with Strasbaugh's 6DS-SP and Westech's 372M polishers. 1995 was therefore the first year of the Integrated Metrology (IM) era in semiconductor manufacturing, and IM formed a paradigm shift in CMP processing.

The main significant advantages realized by the semiconductor manufacturers using the NovaScan IM systems, were:

- Increased polishing tool efficiency
- Faster response and higher sampling rate leading to a significantly better process control
- Shorter manufacturing cycle
- Elimination of test wafers
- Savings of labor and clean room space required for SA metrology tools

All these led to a wide acceptance and fast penetration of the NovaScan IM systems as part of the CMP manufacturing process (with practically all existing and new polishing tool manufacturers and models). However, the close cooperation required between the end-users, the process equipment manufacturers (PEM's) and IM system manufacturers, did pose a lot of challenges and barriers to overcome, both technologically and commercially. Currently, 10 years after the initial introduction of Integrated Metrology to the market, the penetration level for dielectric CMP is close to 100%.

Newer generations of CMP polishers became "dry-in/dry-out", enabling also the less complex IM "dry integration": Wafers are measured in-air, after cleaning and drying, before moving to the output cassette [8]. However, many semiconductor manufacturers continue to select the "wet integration" for the "dry-in/dry-out" polishers. This is primarily because the response time to the polish process is faster and enables effective wafer-to-wafer control. Table 1 below summarizes the main differences between the integration concepts for dielectric CMP.

Wet	Dry
• Complex and more costly • Fastest feedback for CLC and excursions control • Significant reduction of rework in STI w/o over polish • Reduction of Gating Wafers cycle time • 100% pre and post	• Faster and cheaper • Easier application development • Higher sensitivity to STI oxide residues • Recipe compatibility with Stand Alone metrology tools. • 100% pre and post

Table 1. Wet vs. Dry Integrations

Currently all leading polishers are offered with on-board IM tools that enable both excursion control and APC for all CMP processes: ILD, IMD, STI, poly-Si, W and Copper. The significant advancement in IM systems development over the last decade led to systems that are fast enough to measure every wafer, before and after CMP, adding the incoming thickness variations in the CLC models.

The metrology itself significantly evolved from “simple” visible light Reflectometry in the first models to Scatterometry in the latest models with polarized light in a broad spectral range - from DUV to NIR, enabling also small spot size, very high throughput and ability of both wet and dry integration. In the 65 to 45nm technology nodes we expect that all measurements will be performed on arrays (vs. solid pads today) within the dies or on test sites in order to provide the best correlation with actual effects, such as local planarity, on device patterns.

Integration between the IM tool and the CMP polisher has significantly evolved during this period. The first IM tools were installed inside the polishers, but their operation was independent – recipe design, measurement runs, and data collection were separated from the polisher’s computer and with a separate user interface. Currently the integration between the process and the metrology tools is more extensive: all the IM operations are carried out from the polisher’s GUI through SECS/GEM communication. The measurement results are used in real time for CLC, and provide the polishing parameters to the next wafers in the lot.

During this decade, Integrated Metrology has experienced fast growth and major changes in the CMP area: currently over 1500 IM tools are operating in all advanced semiconductor fabs. The application areas have broadened and advanced:

- ☐ From measuring thick ILD layers to measuring single Angstrom residues after STI and Copper polish
- ☐ From solid test sites measured by visible reflectometry to line arrays measured by DUV scatterometry
- ☐ From 2 minutes on 200 mm wafer measured at 5 points to 13 seconds on 300 mm wafer measured at 13 points.
- ☐ From simple SPC to real-time CLC.

Examples of IM tools are presented in figures 2 and 3. IM tool development will continue to meet the new requirements of the next ITRS technology nodes.

Fig. 2 Wet NovaScan 210 integrated onto a Westech 372

Fig. 3 NovaScan 3060 in Dry Factory Interface module

With the introduction of APC methodology and algorithms, Integrated Metrology has moved metrology from its original and historical position of “a non-value added operation” to become an “added-value” operation.

IM based Closed Loop Control (CLC)

Enhancing the Polishing Process by Using Integrated Metrology with CLC

IM tools enable Wafer-to-Wafer and Within-Wafer process control. Closed Loop Control (CLC), utilizing the measurement data (pre- and post-polish) provides real-time adjustment of the CMP process.

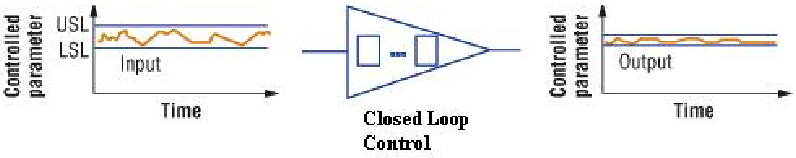


Fig. 4. Closed Loop Control enabling reduction of output variations

CMP processing suffers from a relative fast drift of process parameters (such as removal rate), which requires continuous monitoring of the process performance and data feedback from each wafer to the process controller. The process controller can then dynamically adjust the process conditions for the following wafer, e.g. by adjusting polishing time for every wafer.

The use of classical control theory, advanced filtering methods and extensive accumulated field experience provided a solid basis for the production-reliable CLC option. Sampling rate is very high, as the IM systems measure each wafer, and the process parameters are fed (back) to the next wafer polished. With the new IM tools, enabling 100% pre-and post- measure, the advantages of CLC with the combined feed forward and feedback allow further improvement of productivity and cost of ownership.

The benefits of using real time CLC are [4,5]:

- Improved outgoing CMP quality
- Reduced cycle time in CMP area
- Reduced consumables usage
- Improved polisher utilization and productivity
- Reduced labor
- Decrease test wafer

CLC Results

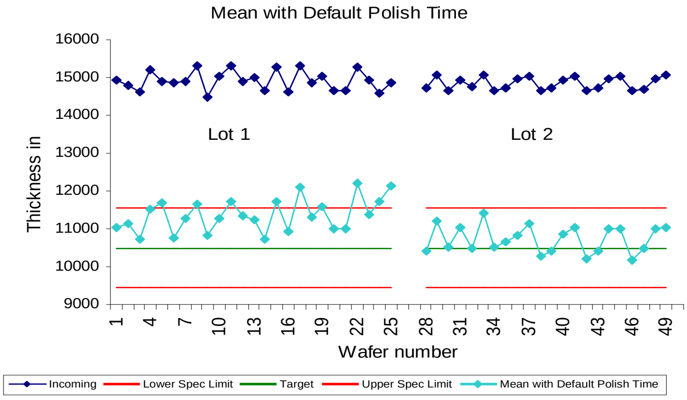


Fig. 5 Open loop control using default polish time

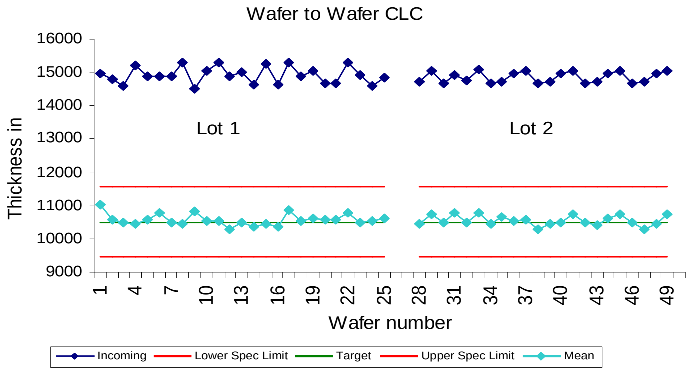


Fig. 6. Closed loop control - polish time adjusting for every wafer.

IM Role in STI CMP

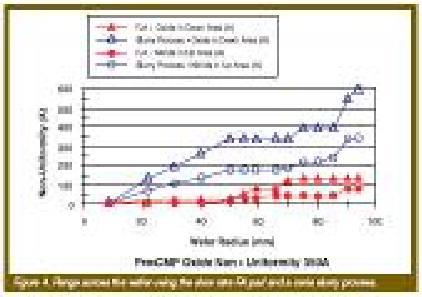
As device geometries continue to shrink, planarity requirements for Shallow Trench Isolation (STI) chemical mechanical planarization are becoming increasingly stringent and process requirements of STI CMP result in a much narrower process window. One of the greatest challenges in STI CMP involves the achievement of planarization uniformity over both the die level and the wafer level. Uniformity requirements vary with device and application, but typically the thickness uniformity across the wafer (within-wafer non-uniformity, or WIWNU) must be <3%. Dishing of the trench oxide must typically be <20-50nm. Accordingly, the quality of an STI process is measured by the control of trench oxide and nitride thickness

A new approach to STI CMP has been developed through the use of Slurry-Free Fixed Abrasive (FA) technology or High Selectivity Slurry (HSS) that is named “Direct STI”, removing the need of reverse etch-back process steps before CMP or the use of "dummy" patterns. Direct STI improves the cost of ownership and reduces the cycle time. Direct STI requires greater control of the CMP process and lower sensitivity to pattern density and feature size. The key advantage of using FA is its selectivity to topography up to (>100:1) and the use of HSS that improves the ability to halt polishing on the nitride stop layer.

There are 2 basic needs for control in STI:

1. Confirm the non-existence of residues (down to 40Å of oxide). Current methods have limited accuracy and require other measurement tools such as TEM, which can be used as limited reference only, because of their destructive nature. The use of enhanced algorithms capabilities in the current Reflectometry tools that measure in production is a more practical option. For absolute accurate residues measurement the “Pre-Post Injection” [13] was developed extending the range of oxide residue measurement significantly down to 4Å dynamic repeatability (3σ) on 40Å residues (figure 8).

2. WIWNU and edge measurements requires the gathering of a large number of measurement points to enable the best CLC algorithms:
    a. Across the wafer edge measurement
    b. Across the die information gathering
    c. 100% pre and post measurement



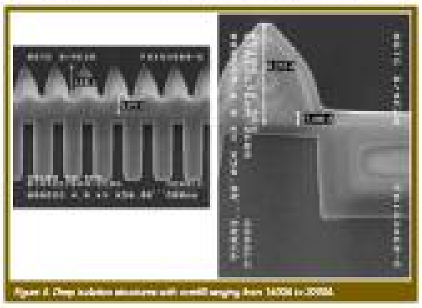


Fig. 7 Thickness range across the wafer using the slow rate FA pad and a Ceria slurry process [12].

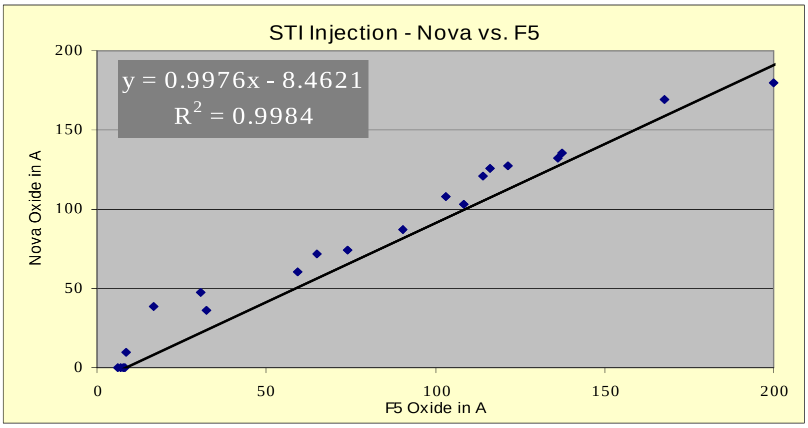


Fig 8. STI residues using injection pre/post vs. F5 Stan Alone

IM role in Copper CMP Process Control

The goal in Copper CMP is to stop the first-step polish on the barrier layer without inducing dishing, erosion and non-uniformity, and then remove the barrier and some dielectric films in the second-step polish. Due to the significant differences between polish rates of copper, barriers, cap layers, oxide and low K materials, dishing of copper pads and erosion of copper line arrays are an inherent part of the polish step output. When IC manufacturers are integrating low-k with cap/hard masks films, it is very important to remove the cap layer but leave the low-k dielectric layer intact. These materials protect the porous and mechanically weak low-k dielectrics from destruction that causes reduction of the overall dielectric constant k (k_{eff}) in the CMP. Therefore, very tight thickness control of the cap layer is needed. CLC by the help of IM can be effectively used for this type of application.

Various methods are being used to overcome these hurdles of copper and low-k. New polish processes involving low down force are being developed to reduce the mechanical stresses on the films during CMP.

Another required capability is a tight control of erosion. Erosion measurements show a strong correlation to the electrical performance of the copper line, and good control of the erosion also reduces the probability of residues in higher metal levels.

Measuring the erosion optically directly in the die area or on special test structures [5] reduces cycle time and eliminates the need for HRP measurements. By measuring erosion with an IM system the next stage of Copper APC is enabled. Fig. 9 shows the correlation between 3 wafers on 3 different pitches: on 0.24 and 0.35 um pitch arrays relative to 1 um array.

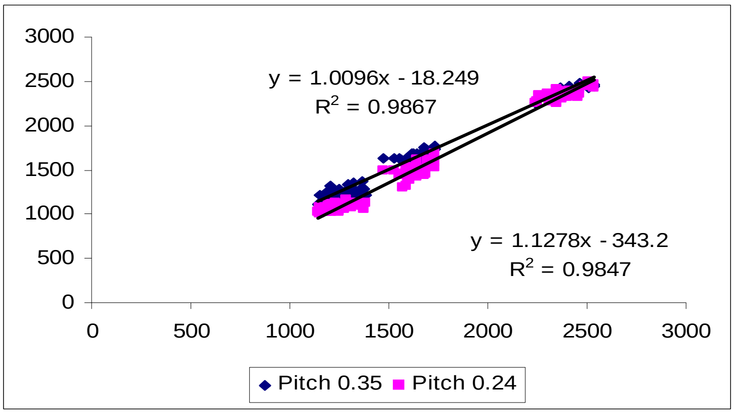
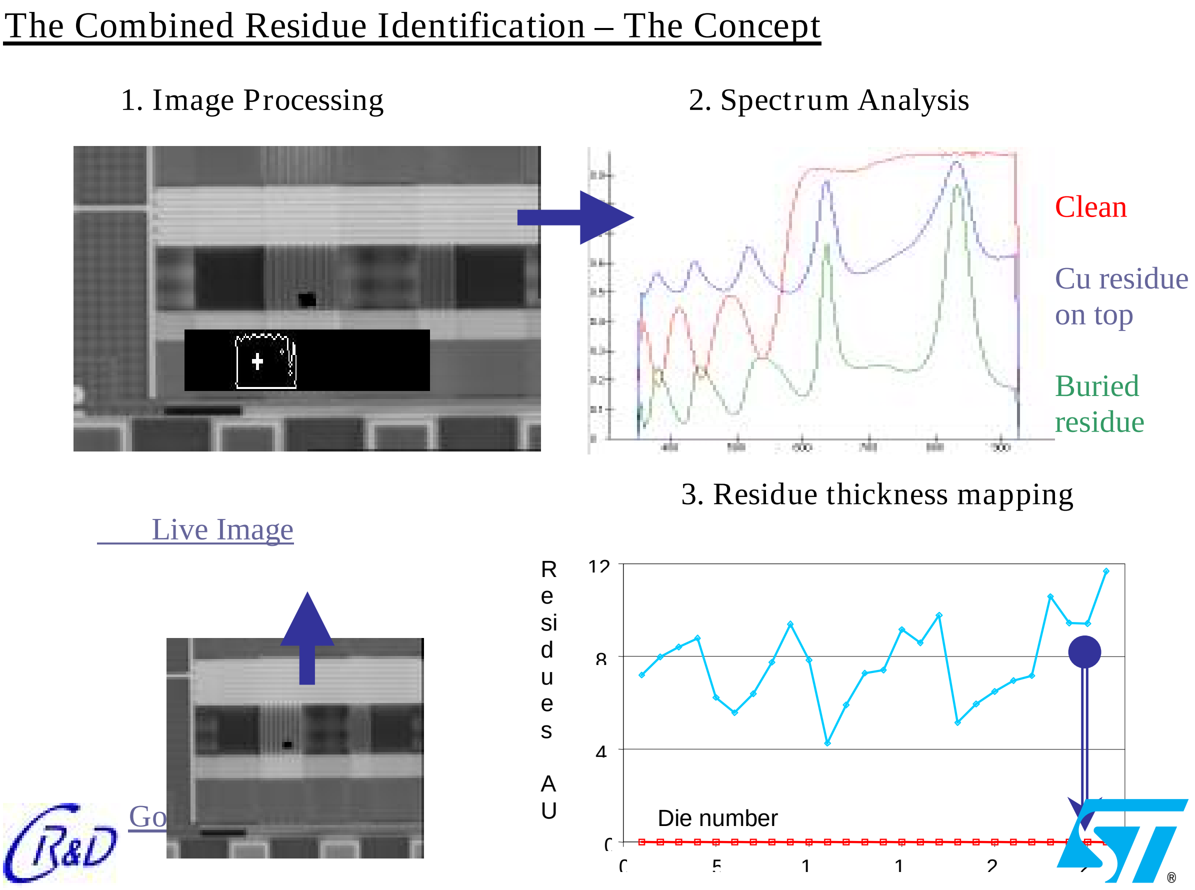


Fig.9. Residues detection and characterization by Integrated Metrology

Newcomers in Copper CMP usually need the detection and determination of residue (copper or barrier) as an important excursion control. The balance in the multiple step copper CMP between over-polishing, leading to dishing and erosion and under-polishing leaving copper/barrier residues is very subtle. This excursion control may be effectively achieved by the same IM system combining image processing and spectrophotometric measurement [5]. Fig 10. above illustrates this method of residues detection and characterization [6,11].



The Combined Residue Identification – The Concept

1. Image Processing

2. Spectrum Analysis

3. Residue thickness mapping

Fig. 10 IM residues detection mode of operation.

Summary

Integrated Metrology and the associated Advanced Process Control technologies have become an inherent part of dielectric and Copper CMP. During the 10 years of its use in production, optical measurement systems and APC algorithms evolved continuously with the increasing requirements of the CMP processing. In parallel, multiple technologies for in-situ measurements and control have been developed as well, complementing to the capabilities of integrated metrology. All will continue to evolve to meet the control criteria as defined in the ITRS for technology nodes of 65 and 45 nm, requirements which pose new challenges for Integrated Process Control primarily for STI and Copper/low-k CMP.

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